Remarks

Reconsideration of this application is requested. By this response to the Office Action claims 1-4 were amended. Claims 5-17 and 19-48 were canceled in a previous response. A listing of claims and the actions taken is included in this amendment. Claims 1-4 and 18 remain in the application.

Objections to the drawings

The Office Action objected to the drawings under 37 CFR 1.83(a). New drawings that include all of the figures appearing on the immediate prior version of the sheet have been properly marked in compliance with 37 CFR 1.121(d).

Objections to claims 1-4 and 18

The Office Action objects to claims 1-4 and 18 under 35 U.S.C. 102(e) as being anticipated by Heidari-Bateni et al. (U.S. 6,618,434).

Claims 1-4

Applicant's amended claim 1 recites first and second multiplication units; and a first multiplexer selectively connectable to supply first and second operands, where in a first configuration the first operand is supplied through a second multiplexer to a first input of the first multiplication unit and the second operand is supplied through a third multiplexer to a first input of the second multiplication unit.

Support for Applicant's amended claim language for claim 1 can be found in at least FIG. 3D that illustrates a first configuration. A first multiplexer 42 (labeled IMP 0) is wide enough to hold and transfer two operands labeled "H" and "L". In accordance with Applicant's claim 1, a multiplexer 42 supplies the operand "H" through a second multiplexer to a first input of the first multiplication unit 50 and the operand "L" through a third multiplexer to a first input of the second multiplication unit 52.

Heidari-Bateni et al. teach a reconfigurable chip having multiple computational elements 250 with fixed or dedicated, application specific circuits designed and having a corresponding logic gate layout to perform a

specific function or algorithm (column 16, lines 52-57). The application specific circuits perform linear operations such as multiplication, addition, finite impulse response filtering (column 16, lines 11-15).

In FIG. 6 Heidari-Bateni et al. teach that input lines 281 may be activated or deactivated by the control lines to the input mux 280 (column 17, lines 9-17). A data interconnect network 240 of varying bit widths is supplied to the input mux 280 to create the configurable and reconfigurable connects (column 17, lines 31-42). Note from FIG. 6 that multiple input muxes 280 supply data to the CU core 260. It is not stated and it cannot be inferred that Heidari-Bateni et al. teach a first multiplexer selectively connectable to supply both the first and second operands to a multiplication unit as claimed in Applicant's claim 1. Accordingly, the relied upon prior reference cannot anticipate Applicant's claim 1 and it is believed that this claim is allowable over the art of record.

Applicant's amended claim 2 recites a fourth multiplexer selectively connectable to supply third and fourth operands, where in the first configuration the third operand is supplied through a fifth multiplexer to a second input of the first multiplication unit and the fourth operand is supplied through a sixth multiplexer to a second input of the second multiplication unit.

Support for Applicant's amended claim 2 is found in the embodiment illustrated in FIG. 3D, where a fourth multiplexer 44 (labeled IMP 1) passes a third operand labeled "H" to a second input of the first multiplication unit 50 and the fourth operand labeled "L" to a second input of the second multiplication unit 52.

Applicant's amended claim 3 recites an adder unit having first and second inputs respectively coupled to outputs of the first and second multiplication units. Support for Applicant's amended claim 3 is found in at least the embodiment illustrated in FIG. 3E, where adder unit 58 has a first input coupled to an output of the multiplication unit 50 and a second input coupled to an output of the multiplication unit 52.

Applicant's amended claim 4 recites the first and second inputs of the adder unit are coupled through seventh and eighth multiplexers to the outputs of the first and second multiplication units. The elements of the claim are at

least supported by the embodiment illustrated in FIG. 3E, where adder unit 58 has a first input coupled through a multiplexer to an output of the multiplication unit 50 and a second input coupled through another multiplexer to an output of the multiplication unit 52.

Claims 2-4 depend, either directly or indirectly, from base claim 1 and are believed allowable over the art of record for at least the same reasons as claim 1.

Claim 18

Applicant's amended claim 18 recites a multiplication block including first and second multiplexers, a multiplication unit having first and second multipliers, and an adder unit, wherein a first configuration instruction to the multiplication block configures the multiplication unit to receive operands from the first and second multiplexers and provide a summed product of the operands at an output, and a second configuration instruction configures the adder unit to receive the operands from the first and second multiplexers and provide a summed value of the operands.

Support for Applicant's claim 18 is found in at least FIGs. 3C and 3E where the output of the adder unit 58 provides a summed product of the operands supplied to multiplication units 50 and 52 in one configuration (FIG. 3E), and a summed value of the operands at the output of the adder unit 58 in another configuration (FIG. 3C).

The Examiner relies on FIG. 7D of Heidari-Bateni et al. to teach A multiplication unit configured to receive first and second operands from first and second multiplexers and provide a summed product of the operands at an output and a second configuration instruction that configures first and second adder units to receive the first and second operands from the first and second multiplexers and provide a summed value of the operands.

The Examiner does not point out the specific output in Heidari-Bateni's FIG. 7D that provides both a summed product in one configuration and a summed value of the operands in another configuration. Further, ADDER 545 does not receive operands from MUX 510i. Accordingly, Applicant's claim 18

cannot be anticipated by the relied upon reference and the rejection should be removed.

Conclusion

The foregoing is submitted as a full and complete response to the Office Action mailed May 6, 2005, and reconsideration of the objections and rejections is requested. It is submitted that claims 1-4 and 18 are now in condition for allowance. Allowance of these claims is earnestly solicited.

Applicants herewith petition the Director of the United States Patent and Trademark Office to extend the time for response to the Office Action dated May 6, 2005, for 2 months. Please charge Deposit Account #50-0221 in the amount of $450.00 for a two month extension. Should it be determined that an additional fee is due under 37 CFR §1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #50-0221.

If the Examiner believes that there are any informalities that can be corrected by an Examiner's amendment, a telephone call to the undersigned at (480) 715-5388 is respectfully solicited.

Respectfully submitted,
Gary N. Lai

Lanny L. Parker
Patent Agent
Reg. No. 44,281

c/o Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026
(503) 264-0967